# CFP-LR4-LL-10KM
## 100 Gb/s CFP LR4 Transceiver

## PRODUCT FEATURES




- Compliant with 100GBASE-LR4
- Support line rates from 103.125 Gbps to 111.81 Gbps
- Integrated LAN WDM TOSA / ROSA for up to 10 km reach over SMF
- CAUI(10x10G) Electrical Interface and 4-lane 25.78Gb/s optical interface
- Duplex LC optical receptacle
- MDIO Interface for module management
- Single 3.3 V power supply
- Case operating temperature range:0°C to 70°C
- Power dissipation < 12W

## APPLICATIONS

- Data Center &100G Ethernet
- ITU-T OTU4

## STANDARD

- Compliant to IEEE 802.3ba
- Compliant to CFP MSA Hardware Specification
- Compliant to CFP MSA Management Interface Specification

## General Description

The LONGLINE CFP LR4 is the optical transceiver module which is a hot pluggable form factor designed for high speed optical networking application. The LONGLINE CFP LR4 is designed for 100 Gigabit Ethernet application and provides 100GBASE-LR4 compliant optical interface, CAUI electrical interface and MDIO module management interface. The LONGLINE CFP LR4 converts 10-lane 10.3Gb/s electrical data streams to 4-lane LAN-WDM 25.78Gb/s optical output signal and 4-lane LAN-WDM 25.78Gb/s optical input signal to 10-lane 10.3Gb/s electrical data streams. This 10-lane 10.3Gb/s electrical signal is fully compliant with IEEE 802.3ba CAUI specification. The high performance Cooled LAN-WDM EA-DFB transmitter and high sensitivity PIN receiver provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant optical interface with IEEE802.3ba 100GBASE-LR4 requirements.

The LONGLINE CFP LR4 contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. Figure 1 shows the functional block diagram of LONGLINE CFP LR4.

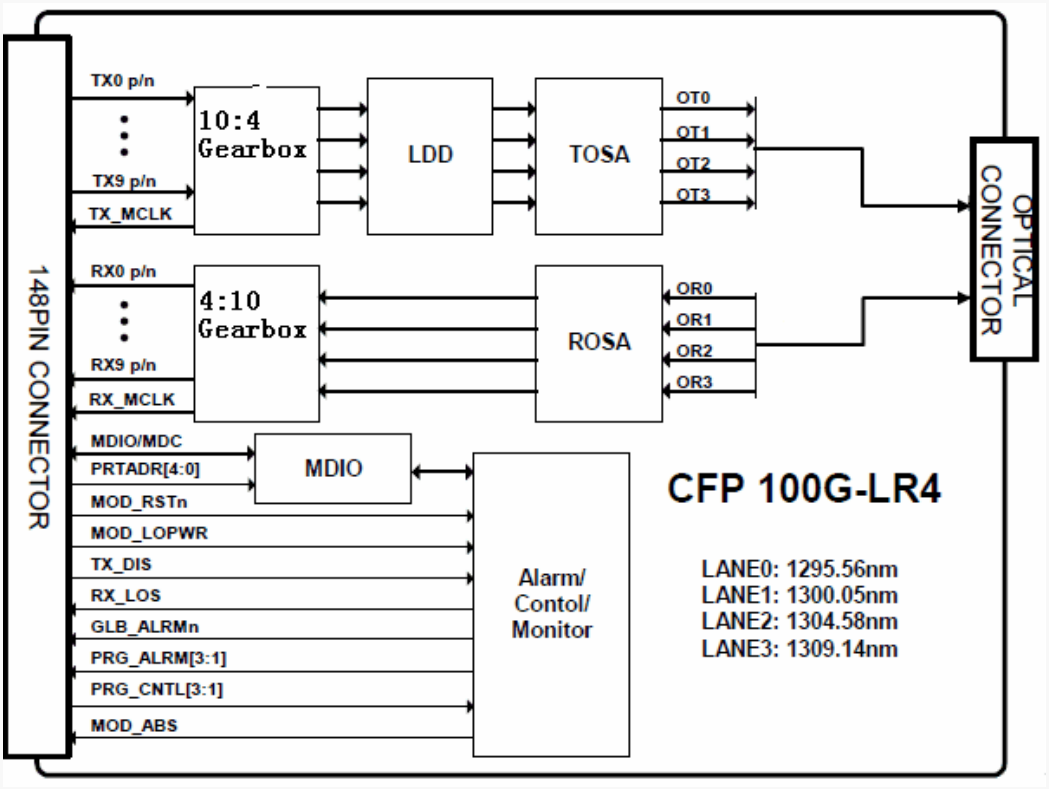



**Figure 1.** **CFP LR4 Optical Transceiver functional block diagram**

**Transmitter**

The transceiver module receives 10-lane 10.3 Gb/s CAUI electrical inputs. The gearbox multiplexes 10-lane electrical signals to 4-lane electrical signals. The multiplexed 4-lane signals are fed to the transmitters. The four transmitters convert 4-lane signals to an optical signal through 4 Laser drivers and Lasers diodes which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each Laser launches optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-LR4 requirements. These 4-lane optical signals will be optically multiplexed into one fiber by 4 to1 Optical WDM MUX which is in the TOSA. The optical output power is held constant by an automatic power control (APC) circuit. The transmitters output can be turned off by TX_DIS hardware signal and/or through MDIO module management Interface.

**Receiver**

The LONGLINE CFP LR4 receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by 1 to 4 optical DE-MUX and fed into each Receiver Optical Sub-Assembly（ROSA）integrated 1:4
optical DE-MUX. The ROSA converts optical signal to electrical signal. The 4-lane regenerated electrical signals are de-multiplex to 10-lane signals by the 4 to 10 gearbox. The 10-lane signals are compliant with IEEE CAUI interface requirements. Each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be launched.

**Table 1 CFP optical transceiver pin descriptions**

| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 1 | 3.3V_GND | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 2 | 3.3V_GND | | |
| 3 | 3.3V_GND | | |
| 4 | 3.3V_GND | | |
| 5 | 3.3V_GND | | |
| 6 | 3.3V | | |
| 7 | 3.3V | | |
| 8 | 3.3V | | |
| 9 | 3.3V | | |
| 10 | 3.3V | | |
| 11 | 3.3V | | |
| 12 | 3.3V | | |
| 13 | 3.3V | | |
| 14 | 3.3V | | |
| 15 | 3.3V | | |
| 16 | 3.3V_GND | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 17 | 3.3V_GND | | |
| 18 | 3.3V_GND | | |
| 19 | 3.3V_GND | | |
| 20 | 3.3V_GND | | |
| 21 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 22 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 23 | GND | | |
| 24 | TX_M CLKn | | TX Monitor Clock Output (Negative) |
| 25 | TX_M CLKp | | TX Monitor Clock Output (Positive) |
| 26 | GND | | |
| 27 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 28 | NUC | | Module Vendor I/O. Must No Connect at host board |

| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 29 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 30 | PRG_CNTL1 | LVCMOS w/ PUR | Programmable Control 1 set over MDIO, M SA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used |
| 31 | PRG_CNTL2 | LVCMOS w/ PUR | Programmable Control 2 set over MDIO, M SA Default: Hardware Interlock LSB,"00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: ≤32W = not used |
| 32 | PRG_CNTL3 | LVCMOS w/ PUR | Programmable Control 2 set over M DIO, M SA Default: Hardware Interlock M SB,"00": ≤8W, "01":≤16W, "10": ≤24W, "11" or NC: ≤32W = not used |
| 33 | PRG_ALRM 1 | LVCM OS | Programmable Alarm 1 set over MDIO, M SA Default: HIPWR_ON, "1": module, power up completed, "0": module not high powered up |
| 34 | PRG_ALRM 2 | LVCM OS | Programmable Alarm 2 set over MDIO, M SA Default: M OD_READY, "1": Ready, "0":not Ready, |
| 35 | PRG_ALRM 3 | LVCM OS | Programmable Alarm 3 set over MDIO, M SA Default: M OD_FAULT, fault detected,1": Fault, "0": No Fault |
| 36 | TX_DIS | LVCM OS w/ PUR | Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled |
| 37 | MOD_LOPWR | LVCM OS w/ PUR | Module Low Power M ode. "1" or NC: module in low power (safe) mode, "0": power- on enabled |
| 38 | MOD_ABS | | Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host |
| 39 | MOD_RSTn | LVCM OS w/ PUR | Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module |
| 40 | RX_LOS | LVCM OS | Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition |
| 41 | GLB_ALRM n | LVCM OS | Global Alarm. “0": alarm condition in any M DIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host |
| 42 | PRTADR4 | 1.2V CM OS | M DIO Physical Port address bit 4 |
| 43 | PRTADR3 | 1.2V CM OS | M DIO Physical Port address bit 3 |
| 44 | PRTADR2 | 1.2V CM OS | M DIO Physical Port address bit 2 |
| 45 | PRTADR1 | 1.2V CM OS | M DIO Physical Port address bit 1 |
| 46 | PRTADR0 | 1.2V CM OS | M DIO Physical Port address bit 0 |
| 47 | M DIO | 1.2V CM OS | Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba) |
| 48 | M DC | 1.2V CM OS | Management Data Clock (electrical specs as per 802.3ae and ba) |
| 49 | GND | | |
| 50 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 51 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 52 | GND | | |
| 53 | NUC | | Module Vendor I/O. Must No Connect at host board |
| 54 | NUC | | Module Vendor I/O. Must No Connect at host board |

| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 55 | 3.3V_GND | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 56 | 3.3V_GND | | |
| 57 | 3.3V_GND | | |
| 58 | 3.3V_GND | | |
| 59 | 3.3V_GND | | |
| 60 | 3.3V | | 3.3V Module Supply Voltage |
| 61 | 3.3V | | |
| 62 | 3.3V | | |
| 63 | 3.3V | | |
| 64 | 3.3V | | |
| 65 | 3.3V | | |
| 66 | 3.3V | | |
| 67 | 3.3V | | |
| 68 | 3.3V | | |
| 69 | 3.3V | | |
| 70 | 3.3V_GND | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 71 | 3.3V_GND | | |
| 72 | 3.3V_GND | | |
| 73 | 3.3V_GND | | |
| 74 | 3.3V_GND | | |
| 75 | 3.3V_GND | | |
| 76 | RX_MCLKp | | RX Monitor Clock Output (Positive) |
| 77 | RX_MCLKn | | RX Monitor Clock Output (Negative) |
| 78 | GND | | |
| 79 | RX0p | HS I/O | Lane 0 Receiver Output (Positive) |
| 80 | RX0n | HS I/O | Lane 0 Receiver Output (Negative) |
| 81 | GND | | |
| 82 | RX1p | HS I/O | Lane 1 Receiver Output (Positive) |
| 83 | RX1n | HS I/O | Lane 1 Receiver Output (Negative) |
| 84 | GND | | |
| 85 | RX2p | HS I/O | Lane 2 Receiver Output (Positive) |
| 86 | RX2n | HS I/O | Lane 2 Receiver Output (Negative) |
| 87 | GND | | |
| 88 | RX3p | HS I/O | Lane 3 Receiver Output (Positive) |

| Pin no. | Name | Type | Description |
|---|---|---|---|
| 89 | RX3n | HS I/O | Lane 3 Receiver Output (Negative) |
| 90 | GND | | |
| 91 | RX4p | HS I/O | Lane 4 Receiver Output (Positive) |
| 92 | RX4n | HS I/O | Lane 4 Receiver Output (Negative) |
| 93 | GND | | |
| 94 | RX5p | HS I/O | Lane 5 Receiver Output (Positive) |
| 95 | RX5n | HS I/O | Lane 5 Receiver Output (Negative) |
| 96 | GND | | |
| 97 | RX6p | HS I/O | Lane 6 Receiver Output (Positive) |
| 98 | RX6n | HS I/O | Lane 6 Receiver Output (Negative) |
| 99 | GND | | |
| 100 | RX7p | HS I/O | Lane 7 Receiver Output (Positive) |
| 101 | RX7n | HS I/O | Lane 7 Receiver Output (Negative) |
| 102 | GND | | |
| 103 | RX8p | HS I/O | Lane 8 Receiver Output (Positive) |
| 104 | RX8n | HS I/O | Lane 8 Receiver Output (Negative) |
| 105 | GND | | |
| 106 | RX9p | HS I/O | Lane 9 Receiver Output (Positive) |
| 107 | RX9n | HS I/O | Lane 9 Receiver Output (Negative) |
| 108 | GND | | |
| 109 | NC | | Not Connected Internally |
| 110 | NC | | Not Connected Internally |
| 111 | GND | | |
| 112 | GND | | |
| 113 | TX0p | HS I/O | Lane 0 Transmitter Input (Positive) |
| 114 | TX0n | HS I/O | Lane 0 Transmitter Input (Negative) |
| 115 | GND | | |
| 116 | TX1p | HS I/O | Lane 1Transmitter Input (Positive) |
| 117 | TX1n | HS I/O | Lane 1 Transmitter Input (Negative) |
| 118 | GND | | |
| 119 | TX2p | HS I/O | Lane 2Transmitter Input (Positive) |
| 120 | TX2n | HS I/O | Lane 2 Transmitter Input (Negative) |
| 121 | GND | | |
| 122 | TX3p | HS I/O | Lane 3 Transmitter Input (Positive) |

| Pin no. | Name | Type | Description |
|---|---|---|---|
| 123 | TX3n | HS I/O | Lane 3Transmitter Input (Negative) |
| 124 | GND | | |
| 125 | TX4p | HS I/O | Lane 4 Transmitter Input (Positive) |
| 126 | TX4n | HS I/O | Lane 4 Transmitter Input (Negative) |
| 127 | GND | | |
| 128 | TX5p | HS I/O | Lane 5 Transmitter Input (Positive) |
| 129 | TX5n | HS I/O | Lane 5 Transmitter Input (Negative) |
| 130 | GND | | |
| 131 | TX6p | HS I/O | Lane 6 Transmitter Input (Positive) |
| 132 | TX6n | HS I/O | Lane 6 Transmitter Input (Negative) |
| 133 | GND | | |
| 134 | TX7p | HS I/O | Lane 7Transmitter Input (Positive) |
| 135 | TX7n | HS I/O | Lane 7 Transmitter Input (Negative) |
| 136 | GND | | |
| 137 | TX8p | HS I/O | Lane 8 Transmitter Input (Positive) |
| 138 | TX8n | HS I/O | Lane 8Transmitter Input (Negative) |
| 139 | GND | | |
| 140 | TX9p | HS I/O | Lane 9 Transmitter Input (Positive) |
| 141 | TX9n | HS I/O | Lane 9 Transmitter Input (Negative) |
| 142 | GND | | |
| 143 | NC | | Not Connected Internally |
| 144 | NC | | Not Connected Internally |
| 145 | GND | | |
| 146 | REFCLKp | | Reference Clock Input (Positive) |
| 147 | REFCLKn | | Reference Clock Input (Negative) |
| 148 | GND | | |

## I. Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Storage Temperature | Ts | -40 | - | 85 | ºC | |
| Relative Humidity | RH | 5 | - | 95 | % | |
| Power Supply Voltage | VCC | -0.3 | - | 4 | V | |
| Signal Input Voltage | | Vcc-0.3 | - | Vcc+0.3 | V | |
| Receive Input Optical Power (Damage threshold) | Pdmg | | | 5.5 | dBm | |

## II. Low Speed Electrical Characteristics

| Parameter | Symbol | Min | Typ. | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply currents and voltages | | | | | | |
| Voltage | Vcc | 3.2 | 3.3 | 3.4 | V | With Respect to GND |
| Supply current | Icc | | | 3.6 | A | |
| Power dissipation | Pwr | | | 12.0 | W | |
| Power dissipation (low power mode) | Plp | | | 2.0 | W | |
| Low speed control and sense signals, 3.3 V LVCMOS | | | | | | |
| Outputs low voltage | VOL | -0.3 | | 0.2 | V | |
| Output high voltage | VOH | Vcc-0.2 | | Vcc+0.3 | V | |
| Input low voltage | VIL | -0.3 | | 0.8 | V | |
| Input high voltage | VIH | 2 | | Vcc+ 0.3 | V | |
| Input leakage current | IIN | -10 | | 10 | μA | |
| Low speed control and sense signals, 1.2 V LVCMOS | | | | | | |
| Outputs low voltage | VOL | -0.3 | | 0.2 | V | |
| Output high voltage | VOH | 1.0 | | 1.5 | V | |
| Input low voltage | VIL | -0.3 | | 0.36 | V | |
| Input high voltage | VIH | 0.84 | | 1.5 | V | |
| Input leakage current | IIN | -100 | | 100 | μA | |

## III. MDIO Management Interface

The LONGLINE CFP LR4 supports the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PORT_ADDR0-4) into the module. The CFP transceiver supports MDIO pages 8000h NVR 1 Based ID registers, 8080h NVR 2 Extended ID registers, 8100h NVR 3 network lane specific registers , and pages A000h CFP module VR 1 registers， A080h MLG VR 1 registers, A200h network lane VR 1 registers， A280h network lane VR 2 registers.
Details of the protocol and interface are explicitly described in CFP MSA Management Interface Specification. Please refer to the specifications for design reference.

| Starting Address in Hex | Ending Address in Hex | Access Type | Allocated Size | Data Bit Width | Table Name and Description |
|---|---|---|---|---|---|
| 0000 | 7FFF | N/A | 32768 | N/A | Reserved for IEEE 802.3 Use. |
| 8000 | 807F | RO | 128 | 8 | CFP NVR 1. Basic ID registers. |
| 8080 | 80FF | RO | 128 | 8 | CFP NVR 2. Extended ID registers. |
| 8100 | 817F | RO | 128 | 8 | CFP NVR 3. Network lane specific registers. |
| 8180 | 81FF | RO | 128 | 8 | CFP NVR 4. |
| 8200 | 83FF | RO | 4x128 | N/A | MSA Reserved. |
| 8400 | 847F | RO | 128 | 8 | Vendor NVR 1. Vendor data registers. |
| 8480 | 84FF | RO | 128 | 8 | Vendor NVR 2. Vendor data registers. |
| 8500 | 87FF | RO | 6x128 | N/A | Reserved by CFP MSA. |
| 8800 | 887F | R/W | 128 | 8 | User NVR 1. User data registers. |
| 8880 | 88FF | R/W | 128 | 8 | User NVR 2. User data registers. |
| 8900 | 8EFF | RO | 12x128 | N/A | Reserved by CFP MSA. |
| 8F00 | 8FFF | N/A | 2x128 | N/A | Reserved for User private use |
| 9000 | 9FFF | RO | 4096 | N/A | Reserved for vendor private use. |
| A000 | A07F | R/W | 128 | 16 | CFP Module VR 1. CFP Module level control and DDM registers. |
| A080 | A0FF | R/W | 128 | 16 | MLG VR 1. MLG Management Interface registers |
| A100 | A1FF | RO | 2x128 | N/A | Reserved by CFP MSA. |
| A200 | A27F | R/W | 128 | 16 | Network Lane VR 1. Network lane specific registers. |
| A280 | A2FF | R/W | 128 | 16 | Network Lane VR 2. Network lane specific registers. |
| A300 | A37F | R/W | 128 | 16 | Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers |
| A380 | A3FFF | RO | 128 | N/A | Reserved by CFP MSA |
| A400 | A47F | R/W | 128 | 16 | Host Lane VR 1. Host lane specific registers. |
| A480 | ABFF | RO | 15x128 | N/A | Reserved by CFP MSA. |
| AC00 | AFFF | R/W | 8x128 | 16 | Common Data Block Registers |
| B000 | BFFF | R/W | 32x128 | 16 | Allocated for OIF MSA-100GLH modules |
| C000 | FFFF | RO | 4x4096 | N/A | Reserved by CFP MSA. |

## IV. Optical Transmitter Characteristics

| Parameter | Symbol | Min | Typ. | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Signaling rate, each lane | | | 25.78125 | | GBd | |
| Lane wavelength（range） | | 1294.53 | 1295.56 | 1296.59 | nm | |
| | | 1299.02 | 1300.05 | 1301.09 | nm | |
| | | 1303.54 | 1304.58 | 1305.63 | nm | |
| | | 1308.09 | 1309.14 | 1310.19 | nm | |
| Rate tolerance | | -100 | | 100 | ppm | From nominal rate |
| Side-mode suppression ratio | SMSR | 30 | | | dB | |
| Total launch power | | | | 10.5 | dBm | |
| Average launch power, each lane | Pavg | -4.3 | | 4.5 | dBm | |
| Extinction Ratio | ER | 4 | 8.2 | | dB | |
| Optical modulation amplitude, each lane (OMA) | OMA | -1.3 | | 4.5 | dBm | |
| Difference in launch power between any two lanes (OMA) | | | | 5 | dB | |
| Transmitter and Dispersion Penalty, each lane | TDP | | | 2.2 | dB | |
| OMA minus TDP, each lane | OMA-TDP | -2.3 | | | dBm | |
| Average launch power of OFF transmitter, each lane | | | | -30 | dBm | |
| Relative Intensity Noise | $RIN_{20}OMA$ | | | -130 | dB/Hz | |
| Transmitter reflectance | | | | -12 | dB | |
| Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3} | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | | | |

## V. Optical Receiver Characteristics

| Parameter | Symbol | Min | Typ. | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Signaling rate, each lane | | | 25.78125 | | GBd | |
| Rate tolerance | | -100 | | 100 | ppm | From normal rate |
| Average receive power, each lane | Pavg | -10.6 | | 4.5 | dBm | |
| Receive power, each lane (OMA) | | | | 4.5 | dBm | |
| Difference in receiver power between any two lanes (OMA) | | | | 5.5 | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Receiver Sensitivity (OMA), each lane | Rsen | | | -8.6 | dBm | 1 |
| Stressed Receiver Sensitivity (OMA), each lane | SRS | | | -6.8 | dBm | |
| Stressed receiver sensitivity test conditions | | | | | | |
| Vertical eye closure penalty, each lane | VECP | | 1.8 | | dB | |
| Stressed sys J2 jitter, each lane | J2 | | 0.3 | | UI | 2 |
| Stressed sys J9 jitter, each lane | J9 | | 0.47 | | UI | 2 |
| Receiver reflectance | | | | -26 | dB | |
| LOS Assert | Plos_on | | -18 | | dBm | |
| LOS Deassert | Plos_off | | -15 | | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

1. Receiver sensitivity (OMA), each lane, is informative.
2. Vertical eye closure penalty, stressed eye J2 Jitter, and stressed eye J9 Jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.