# LONGLINE XFP-LL-80KM

# 10Gb/s 80km XFP Optical Transceiver

## PRODUCT FEATURES


Hot-pluggable XFP footprint

Supports 9.95Gb/s to 11.3Gb/s bit rates

Supports Lineside and XFI loopback

RoHS-6 Compliant (lead-free)

Power dissipation <3.0W

3.3V &1.8V power supply

Maximum link length of 80km

Cooled 1550nm EML and APD Receiver

Full Duplex LC connector

No Reference Clock required

Built-in digital diagnostic functions

Standard bail release mechanism

Case operating temperature range: Commercial: 0°C to +70°C

Industrial: -40°C to +85°

## APPLICATIONS

10GBASE-ZR/ZW 10G Ethernet

80KM 10G Fiber Channel

SONET OC-192 &SDH STM 64

## Ordering information

| Product part Number | Data Rate (Gbps) | Media | Wavelength (nm) | Transmission Distance(km) | Temperature Range (Tcase) (℃) | |
|---|---|---|---|---|---|---|
| XFP-LL-80KM | 10.3125 | Single mode fiber | 1550 | 80 | 0~70 | Commercial |
| XFP-LL-80KM | 10.3125 | Single mode fiber | 1550 | 80 | -40~85 | Industrial |

## Ⅰ. Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | NOTE |
|---|---|---|---|---|---|---|
| Maximum Supply Voltage 2 | Vcc2 | -0.3 | | 3.6 | V | |
| Maximum Supply Voltage 3 | Vcc3 | -0.3 | | 2.0 | V | |
| Storage Temperature | TS | -40 | | 85 | °C | |
| Case Operating Temperature | Tcase | 0 | | 70 | °C | |
| | | -40 | - | 85 | ºC | |

## II. Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | NOTE |
|---|---|---|---|---|---|---|
| Supply Voltage – 1.8V supply | Vcc2 | 1.71 | | 1.89 | V | |
| Supply Voltage – 3.3V supply | Vcc3 | 3.13 | | 3.47 | V | |
| Supply Current – 1.8V supply | Icc2 | | | 250 | mA | |
| Supply Current – 3.3V supply | Icc3 | | | 760 | mA | |
| Module total power | P | | | 3.0 | W | 1 |
| **Transmitter** | | | | | | |
| Input differential impedance | $R_{in}$ | | 100 | | Ω | 2 |
| Differential data input swing | Vin,pp | 120 | | 820 | mV | |
| Transmit Disable Voltage | $V_D$ | 2.0 | | Vcc | V | 3 |
| Transmit Enable Voltage | $V_{EN}$ | GND | | GND+ 0.8 | V | |
| Transmit Disable Assert Time | | | | 10 | us | |
| **Receiver** | | | | | | |
| Differential data output swing | Vout,pp | 340 | 650 | 850 | mV | 4 |
| Data output rise time | $t_r$ | | | 38 | ps | 5 |
| Data output fall time | $t_f$ | | | 38 | ps | 5 |
| LOS Fault | $V_{LOS\ fault}$ | Vcc – 0.5 | | $V_{CCHOST}$ | V | 6 |
| LOS Normal | $V_{LOS\ norm}$ | GND | | GND+0.5 | V | 6 |

**Notes:**

1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 ohms differential termination.
5. These are unfiltered 20-80% values

6. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.

## Ⅲ. Optical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | NOTE |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Output Optical Power | Pf | 0 | | 5 | dBm | |
| Optical Wavelength | λ | 1530 | 1550 | 1570 | nm | |
| Side mode Suppression ratio | SMSR | 30 | | | dB | |
| Optical Extinction Ratio | ER | 8.2 | | | dB | |
| Average Launch power of OFF transmitter | POFF | | | -30 | dBm | |
| Eye Mask Margin | | 30 | | | % | |
| **Receiver** | | | | | | |
| Receiver Sensitivity | $R_{SEN}$ | | | -24 | dBm | 1 |
| Input Saturation Power (Overload) | Psat | -6 | | | dBm | |
| Wavelength Range | $\lambda_C$ | 1270 | | 1610 | nm | |
| Receiver Reflectance | Rrx | | | -27 | dB | |
| LOS De-Assert | LOSD | | | -27 | dBm | |
| LOS Assert | LOSA | -37 | | | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

**Notes:**

1. Measured with BER<$10^{-12}$ @10.3Gbps,$2^{31}$ – 1 PRBS.

# IV. Pin Assignment

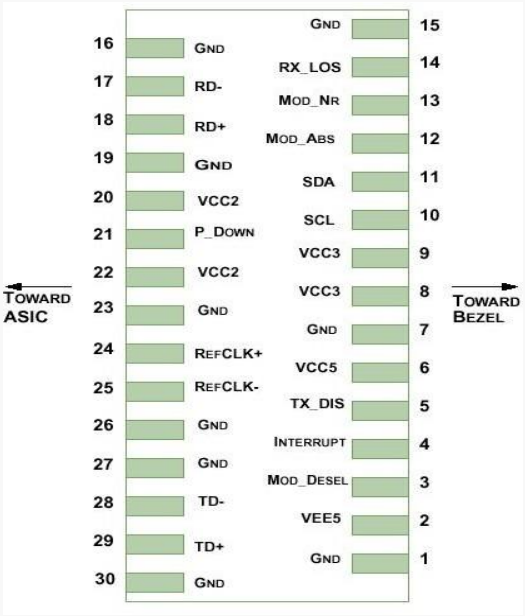


**Diagram of Host Board Connector Block Pin Numbers and Name**

| Pin | Logic | Symbol | Name/Description | NOTE |
|---|---|---|---|---|
| 1 | | GND | Module Ground | 1 |
| 2 | | VEE5 | Optional -5.2 Power Supply – Not required | |
| 3 | LVTTL-I | Mod-Desel | Module De-select; When held low allows the module to respond to 2-wire serial interface commands | |
| 4 | LVTTL-O | Interrupt | Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface | 2 |
| 5 | LVTTL-I | TX_DIS | Transmitter Disable; Transmitter laser source turned off | |
| 6 | | VCC5 | +5 Power Supply – Not required | |
| 7 | | GND | Module Ground | 1 |
| 8 | | VCC3 | +3.3V Power Supply | |
| 9 | | VCC3 | +3.3V Power Supply | |
| 10 | LVTTL-I | SCL | Serial 2-wire interface clock | 2 |
| 11 | LVTTLI/O | SDA | Serial 2-wire interface data line | 2 |
| 12 | LVTTL-O | Mod_Abs | Module Absent; Indicates module is not present. Grounded in the module. | 2 |
| 13 | LVTTL-O | Mod_NR | Module Not Ready; LONGLINE defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX. | 2 |
| 14 | LVTTL-O | RX_LOS | Receiver Loss of Signal indicator | 2 |
| 15 | | GND | Module Ground | 1 |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RD- | Receiver inverted data output | |
| 18 | CML-O | RD+ | Receiver non-inverted data output | |
| 19 | | GND | Module Ground | 1 |

| | | | | |
|---|---|---|---|---|
| 20 | | VCC2 | +1.8V Power Supply | |
| 21 | LVTTL-I | P_Down/RST | Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset | |
| | | | Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle. | |
| 22 | | VCC2 | +1.8V Power Supply | |
| 23 | | GND | Module Ground | 1 |
| 24 | PECL-I | RefCLK+ | Reference Clock non-inverted input, AC coupled on the host board – Not required | 3 |
| 25 | PECL-I | RefCLK- | Reference Clock inverted input, AC coupled on the host board – Not required | 3 |
| 26 | | GND | Module Ground | 1 |
| 27 | | GND | Module Ground | 1 |
| 28 | CML-I | TD- | Transmitter inverted data input | |
| 29 | CML-I | TD+ | Transmitter non-inverted data input | |
| 30 | | GND | Module Ground | 1 |

**Notes:**

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.
3. A Reference Clock input is not required by the XFP-LL-80KM. If present, it will be ignored.

## VI. Digital Diagnostic Functions

As defined by the XFP MSA, LONGLINE XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional

for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.